# METHOD FOR REDUCING A MAGNITUDE OF A RATE OF CURRENT CHANGE OF AN INTEGRATED CIRCUIT

## Abstract

A method for reducing a magnitude of a rate of current change of an integrated circuit is provided. The method uses a plurality of transistors controlled by a finite state machine, such as a counter, to gradually reduce current sourced from a power supply. Further, the finite state machine is controlled by a micro-architectural stage that determines when the integrated circuit needs to be powered down.

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